Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method of designing scan chains in a semiconductor chip by considering fabrication process sensitivities, comprising:
assembling a database of design parameters for the semiconductor chip having fabrication process implications;
selecting one or more of the design parameters for use in designing scan chains on the semiconductor chip;
providing a design model for designing scan chains on the semiconductor chip, based on the selected design parameters, that associates a specific design parameter with a specific scan chain;
employing the design model to create physical scan chain designs for the semiconductor chip.

[c2] 2. The method of claim 1, including employing the design model in a place and route program to create physical scan chain designs for the semiconductor chip.

[c3] 3. The method of claim 1, including analyzing scan chain failures for clustering of scan chain failures by similar content.

[c4] 4. The method of claim 1, including correlating scan chain content back to a process cause based upon said analyzing step to create a list of likely causes of the scan chain failures by using a failure analysis method.

[c5] 5. The method of claim 1, including assembling latches into scan chains using a combination of constraints of location of latches and scan chain length, with an additional constraint of latch type to maximize uniformity of latch type by scan chain.

[c6] 6. The method of claim 1, including assembling latches into scan chains while biasing scan chain routing to constrain the scan chain routing to given restricted interconnect layers of the semiconductor chip.

[c7] 7. The method of claim 6, including dividing scan chains into subsets of scan chains to be routed using restricted interconnect layers of the semiconductor chip, placing a restriction only on subsets of a scan chain rather than on an entire scan chain.

[c8] 8. The method of claim 1, including analyzing specific fabrication process sensitivities of latch cells and specific chip layer connectivity combinations in the semiconductor chip.

[c9] 9. The method of claim 1, including revising the design

model as the fabrication process matures.

[c10] 10. A method of designing scan chains in a semiconductor chip by considering fabrication process sensitivities, comprising:
analyzing specific fabrication process sensitivities of all latch cells and specific chip layer connectivity combinations in the semiconductor chip;
assembling latches into scan chains while using a combination of constraints of location of latches and scan chain length, with an additional constraint of latch type to maximize latch type uniformity by scan chain;
assembling latches into scan chains while biasing scan chain routing to constrain scan chain routing to given restricted interconnect layers of the semiconductor chip;
analyzing scan chain failures for clustering of scan chain failures by similar content;
correlating content back to a process cause based upon said analyzing step to create a list of likely causes of the scan chain failures.

[c11] 11. The method of claim 10, including selecting likely causes of the scan chain failures by using a failure analysis method.

[c12] 12. The method of claim 10, including dividing scan chains into subsets of scan chains to be routed using re-

stricted interconnect layers of the semiconductor chip, placing a restriction only on subsets of a scan chain rather than on an entire scan chain.

[c13] 13. The method of claim 12, including optimizing the steps of dividing of subsets and assigning restricted interconnect layers based on a routability analysis.

[c14] 14. The method of claim 10, including optimizing the step of assembling latches into scan chains while using a combination of constraints to balance scan chain content with routability.

[c15] 15. A method of designing scan chains in a semiconductor chip by considering fabrication process sensitivities, comprising:
assembling latch design parameters which are sensitive to process variation or integrity;
formulating a design model of scan chain design based on the state of the process integrity, wherein certain latch designs having dominant sensitivities are targeted to specific scan chains on the chip;
providing the design model as input parameters to a global placement and wiring program used to physically implement the scan chains;
analyzing test data to determine and isolate systematic yield problems denoted by attributes of a statistically

significant failing population of a specific scan chain.

[c16] 16. The method of claim 15, wherein the step of formulating a design model is based on a current state of process.

[c17] 17. The method of claim 15, wherein the step of formulating a design model is based on a predicted state of process.

[c18] 18. The method of claim 15, including assembling latches into scan chains using a combination of constraints of location of latches and scan chain length constraints, with an additional constraint of latch type to maximize latch type uniformity by scan chain.

[c19] 19. The method of claim 15, including assembling latches into scan chains while biasing scan chain routing to constrain scan chain routing to given restricted interconnect layers of the semiconductor chip.

[c20] 20. The method of claim 19, including dividing scan chains into subsets of scan chains to be routed using restricted interconnect layers of the semiconductor chip, placing a restriction only on subsets of a scan chain rather than on an entire scan chain.

[c21] 21. The method of claim 15, including analyzing specific

fabrication process sensitivities of latch cells of the semiconductor chip and specific chip layer connectivity combinations in the semiconductor chip.

[c22] 22. The method of claim 15, including revising the design model as the fabrication process matures.

[c23] 23. The method of claim 15, wherein the step of assembling scan chain parameters include parameters of layer usage, which layer dominates a particular type of latch, via usage, location on chip, scan chain length including latch count and wire length, critical area, redundant versus single elements such as vias, adjacent shapes, voltage domain, clock domain distribution, latch types and non-latch circuit element types.

[c24] 24. The method of claim 23, wherein the non-redundant elements include vias, voltage domain, clock domain distribution, and latch type.

[c25] 25. The method of claim 15, including creating sub-segments of individual scan chains, with each sub-segment having specific design sensitivities.

[c26] 26. The method of claim 15, including extracting fail probabilities using a statistical analysis from the passes and fails of scan chains, even when those scan chains do not consist of only one latch type and do not exist on

only one metal layer.